UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,375	12/31/2003	Eric D. Blom	08211/0200346-US0/P05774	4891

38845 7590 11/16/2005

DARBY & DARBY P.C.
P.O. BOX 5257
NEW YORK, NY 10150-5257

EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

Office Action Summary	Application No.	Applicant(s)	
	10/750,375	BLOM, ERIC D.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10,12,15-19 and 23* is/are allowed.

6)☒ Claim(s) *1-6 and 20-22* is/are rejected.

7)☒ Claim(s) *7-9,11,13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

The drawings are objected to because it appears that the connecting dot between the drain terminal of M10 and PBIAS line should not be there in Fig. 5. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 3 is objected to because of the following informalities: Claim 3, lines 15 and 17-18, the recitation "the first current source" appears to be --the first current source circuit--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 and 20-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Cowles (US 6,700,416 B2).

Regarding claim 1, Cowles discloses in Fig. 5, a tri-level decoder circuit (col. 7, lines 23+) comprising:

a first decoder circuit (M1, M2, M4, M5) that is coupled between an input node (INPUT) and a first output node (LRO), wherein the first decoder circuit includes:

a first switch circuit (M2) that is coupled to the input node; and

a first current mirror circuit (M4, M5) that is coupled between the first switch circuit and the first output node; and

a second decoder circuit (M2, M3, M5, M6) that is coupled between the input node and a second output node (HRO); and

a current source circuit (M1) coupled to the first output node.

Regarding claim 2, Cowles discloses in Fig. 5, a tri-level decoder circuit (col. 7, lines 23+) comprising:

a first decoder circuit (M1, M2, M4, M5) that is coupled between an input node (INPUT) and a first output node (LRO), wherein the first decoder circuit includes:

a first switch circuit (M2) that is coupled to the input node; and

a first current mirror circuit (M4, M5) that is coupled between the first switch circuit and the first output node; and

a second decoder circuit (M2, M3, M5, M6) that is coupled between the input node and a second output node (HRO),

wherein the first current mirror circuit is configured to:

receive a first switch current (current across M2) from the first switch circuit; and

reflect the first switch current to provide a first reflected current at the first output node in accordance with a ratio that is greater than one-to-one (col. 7, lines 58+).

Regarding claim 3, Cowles discloses in Fig. 5, a tri-level decoder circuit (col. 7, lines 23+) comprising:

a first decoder circuit (M1, M2, M4, M5) that is coupled between an input node (INPUT) and a first output node (LRO), wherein the first decoder circuit includes:

a first switch circuit (M2) that is coupled to the input node; and

a first current mirror circuit (M4, M5) that is coupled between the first switch circuit and the first output node; and

a second decoder circuit (M2, M3, M5, M6) that is coupled between the input node and a second output node (HRO),

wherein the first decoder circuit further includes a first current source circuit (M7) coupled to the first switch circuit (M2), the first current source circuit (M7) and the first current mirror circuit (M4, M5) are separate circuit elements, and

wherein the first switch circuit is configured to:

if a control voltage exceeds a low threshold (logic High), reduce a resistance (since M2 is ON) between a first port (drain of M5) of the first current mirror circuit and the first current source circuit;

else (logic Low)

isolate (since M2 is OFF) the first port of the first current mirror circuit from the first current source circuit.

Regarding claim 4, Cowles discloses in Fig. 5, that the first current source circuit comprises at least one of a transistor (M7) or a resistor.

Regarding claim 5, Cowles discloses in Fig. 5, that that the first decoder circuit further includes another current source circuit (M7) coupled to the first switch circuit.

Regarding claim 6, Cowles discloses in Fig. 5, that the first decoder circuit further comprises: a first current branch (M5, M2, M7) including the other current source circuit (M7) and the first switch circuit; and a second current branch (M4, M1) including the current source circuit (M1) and the output node (LRO), and wherein the first current mirror circuit (M4, M5) includes at least one component in each of the first (M5) and second (M4) current branches.

Regarding claim 20, Cowles discloses in Fig. 5, a tri-level decoder circuit, comprising:

means for comparing a voltage (M1, M2) to a first threshold (REF1);

means for comparing the voltage (M2, M3) to a second threshold (REF2);

means for providing a current (M5) in response to the first threshold comparison; and

means for reflecting the current (M4) to provide another current.

Regarding claim 21, Cowles discloses in Fig. 5, a tri-level decoder circuit, comprising:

a first decoder circuit (M1, M2, M4, M5) that is coupled to an input node (INPUT) and a first output node (LRO), wherein the first decoder circuit includes:

a first switch circuit (M2) that is coupled between the input node and a first switch node (drain of M2);

a first current mirror circuit (M4, M5), including:

a first transistor (M5) having at least a gate, a drain, and a source, wherein the drain of the first transistor is coupled to first switch node (drain of M2), and wherein the gate of the first transistor is coupled to the drain of the first transistor; and

a second transistor (M4) having at least a gate, a drain, and a source, wherein the gate of the second transistor is coupled to the gate of the first transistor, and wherein the drain of the second transistor is coupled to the first output node (LRO); and

a second decoder circuit (M2, M3, M5, M6) that is coupled to the input node and a second output node (HRO).

Regarding claim 22, Cowles discloses in Fig. 5, a tri-level decoder circuit, comprising:

a first decoder circuit (M1, M2, M4, M5) that is coupled to an input node (INPUT) and a first output node (LRO), wherein the first decoder circuit includes:

a first switch circuit (M2) that is coupled between the input node and a first switch node (drain of M2); and

a first current mirror circuit (M4, M5) having at least: an input that is coupled to the first switch node (drain of M2), and an output that is coupled to the first output node (LRO); and

a second decoder circuit (M2, M3, M5, M6) that is coupled to the input node and a second output node (HRO).

Allowable Subject Matter

Claim 10, 12, 15-19, and 23 would be allowable if the claim objections are corrected.

Claims 7-9, 11, 13, and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

the best prior art of record, Cowles, taken alone or in combination of other references, does not teach or fairly suggest a tri-level decoder circuit comprising, among other things, a wherein the driver circuit is configured such that if the input node does not receive a driving input signal, the driver circuit actively drives the control node (claims 7, 10); the second decoder circuit includes a second switch circuit coupled to the input node (claims 11 and 12); the first decoder circuit further comprises a non-linear filter circuit (claims 13, 15, 16, and 23); and first, second, third, and fourth current source circuit (claims 17), as set forth in the claims.

Response to Arguments

Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Timothy Callahan can be reached on (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER